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Claims

1. Stereo demultiplexer receiving a frequency demodulated stereo-multiplex signal ($m(t)$) which comprises at least a stereo-difference signal ($m_d(t)$), a stereo-sum signal ($m_s(t)$) and a pilot carrier, comprising a PLL-circuit (4) to recover the pilot carrier and/or at least one harmonic thereof to perform an amplitude demodulation, **characterized in that** said PLL-circuit (4) receives the sampling rate decimated stereo-sum signal ($m_s(t)$) as input signal, which is sampling rate decimated by a decimation factor of D.

2. Stereo demultiplexer according to claim 1, **characterized in that** said sampling rate decimated stereo-sum signal ($m_s(t)$) is further sampling rate decimated by a decimation factor of E before said PLL-circuit (4) receives it as input signal.

3. Stereo demultiplexer according to claim 1 ~~or 2,~~ **characterized in that** said PLL-circuit (4) outputs a recovered pilot carrier which is interpolated so that it has a sampling rate equal to that of the frequency demodulated stereo-multiplex signal ($m(t)$).

4. Stereo demultiplexer according to claim 3, **characterized in that** D-1 or (E·D)-1 interpolated pilot carrier values ($y(k/D + 1)$, ..., $y(k/D + (D-1))$) and one calculated pilot carrier value ($y(k/D)$) are alternately output.

5. Stereo demultiplexer according to claim 4, **characterized in that** said interpolation within the PLL-circuit (4) is performed on basis of a prediction starting at said calculated pilot carrier value.

6. Stereo demultiplexer according to claim 5, **characterized by**
   - a PLL (7, 8, 9, 10, 11, 12) within the PLL-circuit (4) which outputs a phase signal, and
   - a first sinus calculation unit (14) which outputs said one calculated pilot carrier value ($y(k/D)$) on basis of said phase signal.

7. Stereo demultiplexer according to claim 6, **characterized by**
   - second to D^{th} or $(E{\cdot}D)^{th}$ sinus calculation units (15_1, ..., 15_{D-1}) each of which outputs one of said D-1 or (E·D)-1 interpolated pilot carrier values (y(k/

D + 1), ..., y(k/D + (D-1))) on basis of said phase signal and a respective added phase shift value.

8. Stereo demultiplexer according to claim 6 ~~or 7~~, **characterized by**

- a third multiplier (13) which multiplies said phase signal with a factor of 2 before it is input to said first sinus calculation unit (14) and/or a respective second to D^{th} or $(E \cdot D)^{th}$ sinus calculation unit (15_1, ..., 15_{D-1}) via a respective second to D^{th} or $(E \cdot D)^{th}$ adder (16_1, ..., 16_{D-1}) which adds said respective phase shift value so that the 2^{nd} harmonic of the pilot carrier is generated.

9. Stereo demultiplexer according to ~~anyone of claims~~ claim 6 ~~to 8~~, **characterized in that** said PLL (7, 8, 9, 10, 11, 12) comprises

- a first multiplier (7) receiving samples of the stereo-sum signal (x(k)) as multiplicant at a first input,
- a filter (8) receiving the output signal of said first multiplier (7),
- a second multiplier (9) multiplying said output signal of said filter (8) with a PLL gain (PLL_loop_gain),
- a first adder (11) receiving said output signal of said second multiplier (9) at a first input as a first summand, a constant representing the product of the pilot carrier frequency (ω_{pil}) and the sampling periode(T) at a second input as a second summand, and a delayed phase signal which is the output signal of said first adder (11) at a third input as a third summand,
- a delay element (12) receiving said phase signal of said first adder (11) and supplying said delayed phase signal to said third input of said first adder (11), and
- a cosinus calculation unit (10) receiving the phase signal of said first adder (11) and supplying its output signal as multiplier to a second input of said first multiplier (7).